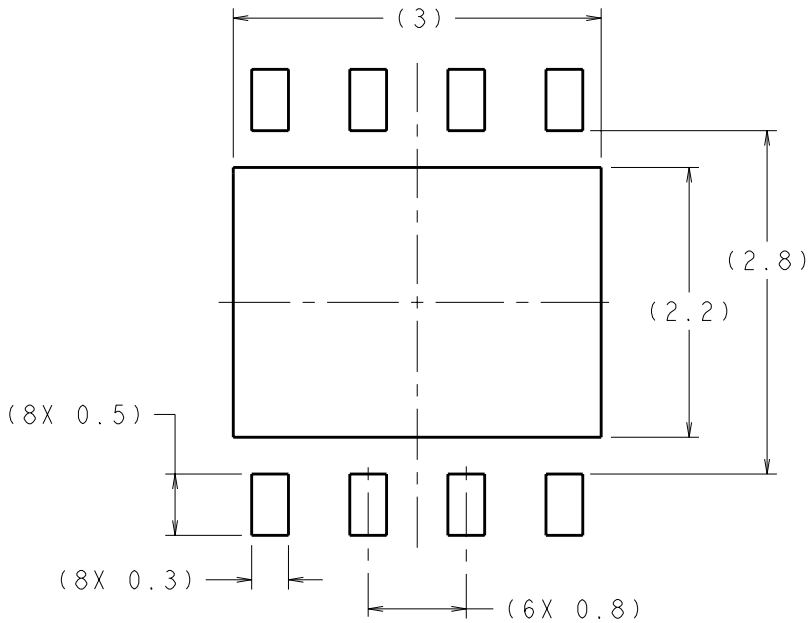
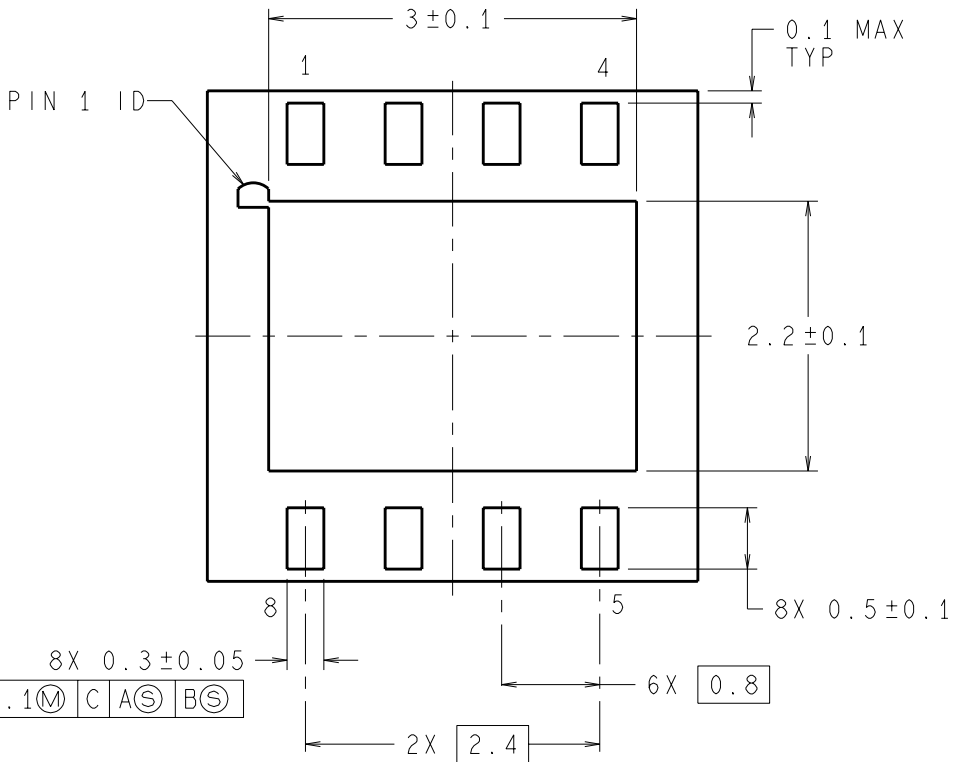
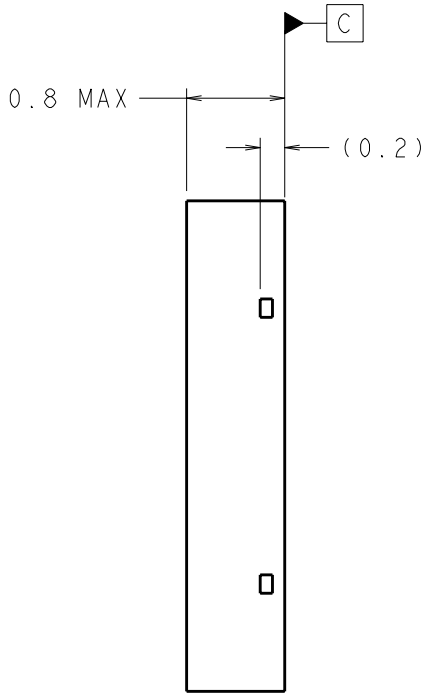
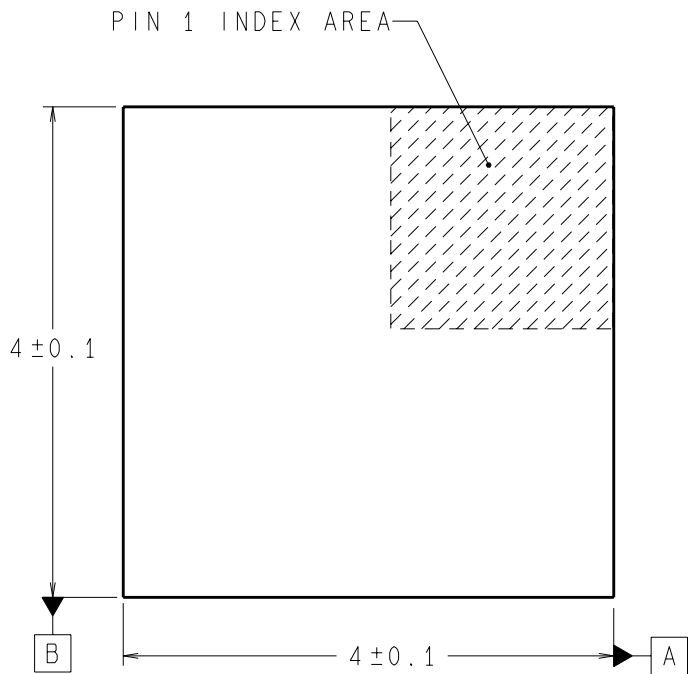


REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	12443	04/27/2000	SN/TL/AL

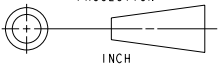


RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS



8X 0.3 ± 0.05	8X 0.5 ± 0.1	6X 0.8	2X 2.4
0.1	C	A	B

- NOTES: UNLESS OTHERWISE SPECIFIED
- STANDARD LEAD FINISH TO BE 5.08 MICROMETERS MINIMUM LEAD/TIN (SOLDER) ON COPPER.
 - NO JEDEC REGISTRATION AS OF APRIL 2000.

APPROVALS		DATE		 <i>National Semiconductor</i> 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	<i>N. SANTHIRAN & TL</i>		04/27/2000		
DFTG. CHK.	<i>MARTA SUCHY</i>		04/27/2000	LLP, PLASTIC, DUAL, 4 X 4 X 0.75 mm BODY, 8 LD, 0.8 mm PITCH	
ENGR. CHK.	<i>ANTHONY LAW</i>		04/27/2000		
 PROJECTION INCH [MM]		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	C	(SC)MKT-LDC08A	A
DO NOT SCALE DRAWING				SHEET 1 of 1	